UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,371	09/16/2003	Katsunori Yamazaki	116573	9410

25944 7590 09/06/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
XIAO, KE	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,371	YAMAZAKI, KATSUNORI	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/6/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 7 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yamazaki (JP 06-027899).

Regarding independent **Claim 1**, Yamazaki teaches an electro-optical device including a plurality of scanning lines and a plurality of data lines, which are wired to cross the scanning lines (Yamazaki, Fig. 1 elements X1-X6 and Y1-Y6), comprising:

electrodes which are wired to cross the data lines and are capacitively coupled with the data lines (Yamazaki, Fig. 1 elements Y1-Y6);

comparison circuits that compare signal levels generated in the electrodes to a predetermined level to output and amount of change in the signal levels (Yamazaki, Fig. 17 elements Vin, Vref and Vout); and

logic circuits that add the amount of change in the signal levels output from the comparison circuits to the signal levels supplied to each scanning line (Yamazaki, Fig. 17 element Vin, Vref, Vout and 176-178).

Regarding **Claim 3**, Yamazaki further teaches the comparison circuit being inversion logic circuit, in which a predetermined bias level is applied to input terminals

(Yamazaki, Fig. 17 an Op-Amp is an inversion logic circuit and the predetermined bias level is Vin and Vref).

Regarding **Claim 7**, Yamazaki further teaches an electronic apparatus comprising the electro-optical device of Claim 1 (Yamazaki, Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (JP 06-027899) in view of the Applicant's Admitted Prior Art (AAPA).

Regarding independent **Claim 2**, Yamazaki teaches an electro-optical device (Yamazaki, Fig. 1) including:

a plurality of scanning lines (Yamazaki, Fig. 1 elements Y1-Y6);

a scanning line driving circuit that supplies to each of the scanning lines a scanning signal which is set to be at a selection level and a non-selection level corresponding to a selection period and a non-selection period of each scanning line (Yamazaki, Fig. 9);

a plurality of data lines which are wired to cross the scanning lines (Yamazaki, Fig. 1 elements X1-X6);

a data line driving circuit that supplies to each of the data lines a data signal on the basis of display data; and

pixels provided in portions where the scanning lines cross the data lines and driven on the basis of the scanning signals and the data signals (Yamazaki, Fig. 9),

the electro-optical device comprising:

electrodes which are wired to cross the data lines and are capacitively coupled with the data lines (Yamazaki, Fig. 1 elements X1-X6 and Y1-Y6);

comparison circuits that compare signal levels generated in the electrodes to a predetermined level to output an amount of change in the signal levels (Yamazaki, Fig. 17 Vref, Vin and Vout); an

logic circuits that add the amount of change in the signal levels output from the comparison circuit to the selection level (Yamazaki, Fig. 17 elements 176-178).

Yamazaki fails to teach that the data signals are pulse width is modulated on the basis of display data. The AAPA teaches that it is well known in the art to use pulse width modulated data signals based on display data (AAPA, Col. 1 paragraph [0008]). It would have been obvious to one of ordinary skill in the art at the time of the invention to use pulse width modulation as taught by the AAPA in the display device of Yamazaki in order to further enhance the control of gray scale images.

Regarding **Claim 4**, Yamazaki further teaches the logic circuits not add the amount of change in the signal levels output from the comparison circuits at an early state of the selection period to the selection level (Yamazaki, Fig. 17 feedback op-amps always have a delay therefore it can be considered not an early state).

Regarding independent **Claim 5**, Yamazaki teaches a method of driving an electro-optical device including a plurality of scanning lines (Yamazaki, Fig. 1 element Y1-Y6), a scanning line driving circuit that supplies to each of the scanning lines a scanning signal which is set to be at a selection level and a non-selection level corresponding to a selection period and a non-selection period of each scanning line (Yamazaki, Fig. 9), a plurality of data lines which are wired to cross the scanning lines, a data line driving circuit that supplies to each of the data lines a data signal on the basis of display data (Yamazaki, Fig. 1 element X1-X6), and pixels provided in portions where the scanning lines cross the data lines and driven on the basis of the scanning signals and the data signals (Yamazaki, Fig. 1 element X1-X6 and Y1-Y6), the method comprising:

wiring electrodes to cross the data lines and capacitively coupling the electrodes with the data line (Yamazaki, Fig. 1 element Y1-Y6);

comparing signal levels generated in the electrodes to a predetermined level to output an amount of change in the signal levels (Yamazaki, Fig. 17 elements Vref, Vin and Vout); and

Yamazaki fails to teach that the data signals are pulse width is modulated on the basis of display data. The AAPA teaches that it is well known in the art to use pulse width modulated data signals based on display data (AAPA, Col. 1 paragraph [0008]). It would have been obvious to one of ordinary skill in the art at the time of the invention to use pulse width modulation as taught by the AAPA in the display device of Yamazaki in order to further enhance the control of gray scale images.

Yamazaki additionally teaches adding the amount of change in the signal levels to the selection level (Yamazaki, Fig. 17 elements 176-178).

Regarding independent **Claim 6**, Yamazaki teaches a circuit for driving an electro-optical device (Yamazaki, Fig. 1) including:

a plurality of scanning lines (Yamazaki, Fig. 1 elements X1-X6 and Y1-Y6);

a scanning line driving circuit that supplies to each of the scanning lines a scanning signal which is set to be at a selection level and a non-selection level corresponding to a selection period and a non-selection period of each scanning line (Yamazaki, Fig. 9);

a plurality of data lines which are wired to cross the scanning lines (Yamazaki, Fig. 1 elements X1-X6);

a data line driving circuit that supplies to each of the data lines a data signal on the basis of display data, and pixels provided in portions where the scanning lines cross the data lines and driven on the basis of the scanning signals and the data signals (Yamazaki, Fig. 1 elements X1-X6),

Yamazaki fails to teach that the data signals are pulse width is modulated on the basis of display data. The AAPA teaches that it is well known in the art to use pulse width modulated data signals based on display data (AAPA, Col. 1 paragraph [0008]). It would have been obvious to one of ordinary skill in the art at the time of the invention to use pulse width modulation as taught by the AAPA in the display device of Yamazaki in order to further enhance the control of gray scale images.

Yamazaki additionally teaches

the circuit comprising electrodes which are wired to cross the data lines and are capacitively coupled with the data lines (Yamazaki, Fig. 1 elements X1-X6 and Y1-Y6);

the circuit comparing signal levels generated in the electrodes to a predetermined level to output an amount of change in the signal levels (Yamazaki, Fig. 17 elements Vref, Vin and Vout); an

the circuit adding the amount of change in the signal levels output from the comparison circuit to the selection level (Yamazaki, Fig. 17 element 176-178).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571) 272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

August 31st, 2006 - kx -

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER